

## Proposal for ETF erratum 350 on configurations.

### In 13.1, REPLACE:

As evidenced by the **config-endconfig** syntax, the config is a design element, similar to a module, which exists in the Verilog namespace. The config contains a set of rules which are applied when searching for a source description to *bind* to a particular instance of the design.

### WITH:

A config is a design element containing a set of rules which are applied when searching for a source description to *bind* to a particular instance in the design. The config definition is enclosed between the **config-endconfig** keywords. The identifier following the keyword **config** is the name of the config.

### In 13.3, REPLACE:

The syntax for configurations is shown in 13.3.1.

### WITH:

The syntax for configurations is shown in 13.3.1. A config shall not appear in a Verilog source description. It shall appear only in a *library map file* (see 13.2.1) or *config file*. The term *config file* is used to avoid confusion when the file contains only configs with no library mapping information.

The library map file or config file has a syntax which is distinct from the syntax of Verilog source files. It uses some keywords which are not considered keywords in Verilog HDL (**cell**, **config**, **design**, **endconfig**, **include**, **instance**, **liblist**, **library**, **use**). A config can still reference a cell name that matches a library map file keyword by using an escaped identifier (see 2.7.1).

### In 13.4.4, REPLACE:

In each of the three preceding strategies, the binding rules can either be specified via a config, or the default rules (from the library map file) can be used. In the single-pass use-models, the config can be specified by including its source description file on the command line. In the case where the config includes a design statement, then the specified cell shall be the top-level module, regardless of the presence of any uninstantiated cells in the rest of the source files. When using a separate compilation tool, the tool which actually does the binding only needs to be given the *lib.cell* specification for the top-level cell(s) and/or the config to be used. In this strategy, the config itself shall also be precompiled.

### WITH:

In each of the three preceding strategies, the binding rules can either be specified via a config, or the default rules (from the library map file) can be used. In the single-pass use-models, the config can be specified by **defining it in the pre-defined library map file, or by specifying a config file including its source description file** on the command line. In the case where the config includes a design statement, then the specified cell shall be the top-level module, regardless of the presence of any uninstantiated cells in the **rest of the Verilog** source files. When using a separate compilation tool, the tool which actually does the binding only needs to be given the *lib.cell* specification for the top-level cell(s) and/or the config to be used. In this strategy, the config itself **shall can** also be precompiled **from a config file**.

**NOTE:** If a tool defines a command line option to specify a library map file to be read, it is recommended that `-libmap` be used. If a tool defines a different command line option to specify a config file to be compiled, it is recommended that `-vconfig` be used. If a tool automatically looks for a file with a specific filename to read as the pre-defined library map file, it is recommended that the filename `lib.map` be used. If a tool uses a filename suffix to distinguish that a file being compiled is a config file, it is recommended that the suffix `cfg` be used. These recommendations are intended to encourage consistent behavior among tools.

In Annex A, under “Formal syntax definition”, replace:

The formal syntax of Verilog HDL is described using Backus-Naur Form (BNF).

**WITH:**

The formal syntax of Verilog HDL is described using Backus-Naur Form (BNF). **The syntax of Verilog HDL source is derived from the starting symbol `source_text`. The syntax of a library map file is derived from the starting symbol `library_text`.**

In Annex B, under “List of keywords”, REPLACE:

An escaped identifier shall not be treated as a keyword.

**WITH:**

An escaped identifier shall not be treated as a keyword.

**These are the keywords for Verilog HDL:**

From the Verilog HDL keyword list, DELETE:

**cell config design endconfig incdir include instance liblist library use**

After the Verilog HDL keyword list, ADD:

**These are the keywords for a library mapping file:**

**cell config default design endconfig include instance liblist library use**

(Note that **default** appears in the library mapping file keywords, but is not removed from the Verilog HDL keywords. It is a keyword in both. The keyword **incdir** is removed from the Verilog HDL keywords, but is not added to the library mapping file keywords. This is because the syntax does not appear to require reserving **incdir** because it always appears after a hyphen (and the BNF does not contain a space to indicate that it is a separate token). However, it could still be added to the list of library mapping file keywords if desired.)