

Hi, All -

Based previous ETF discussions, an updated ETF-9 proposal is shown below.

Regards - Cliff

PROPOSAL: Add a new 4.6 subsection with wording as follows:

4.6 Assignments and truncation

If the width of the right-hand side (RHS) expression is larger than the width of the left-hand side (LHS) in an assignment, the MSBs of the RHS expression will always be discarded to match the size of the LHS. Compliant Verilog simulators are not required to warn or report any errors related to assignment size-mismatch or truncation. Truncating the sign bit of a signed expression, may change the sign of the result.

Example:

```
reg          [5:0] a;
reg signed [4:0] b;

initial begin
    a = 8'hff; // After the assignment, a = 6'h3f
    b = 8'hff; // After the assignment, b = 5'h1f
end
```

Example:

```
reg          [0:5] a;
reg signed [0:4] b, c;

initial begin
    a = 8'sh8f; // After the assignment, a = 6'h0f
    b = 8'sh8f; // After the assignment, b = 5'h0f
    c = -113;   // After the assignment, c = 15
end
// 1000_1111 = (-'h71 = -113) truncates to ('h0F = 15)
```

Example:

```
reg          [7:0] a;
reg signed [7:0] b;
reg signed [5:0] c, d;

initial begin
    a = 8'hff;
    c = a;      // After the assignment, c = 6'h3f
    b = -113;
    d = b;     // After the assignment, d = 6'h0f
end
```