

```
// Example in section 12.4.2 (reformatted and comments added)
module test;
  parameter p = 0, q = 0;
  wire      a, b, c;

  //-----
  // Code to either generate a ul.g1 instance or no instance.
  // The ul.g1 instance of one of the following gates
  // (and, or, xor, xnor) is generated if
  // {p,q}={1,0}, {1,2}, {2,0}, {2,1}, {2,2}, {2,default}
  //-----
  if      (p == 1)
  if      (q == 0) begin : ul
    and g1 (a, b, c);           // if p,q=1,0 - and  test.ul.g1 ...
  end
  else if (q == 2) begin : ul
    or  g1 (a, b, c);           // if p,q=1,2 - or   test.ul.g1 ...
  end
  // else added to terminate "if (q==0)" if-statement
  else ;                         // if p=1 && q!=0 or 2, no inst
  else if (p == 2)
  case (q)
    0, 1, 2: begin : ul
      xor g1 (a, b, c); // if p==2 && q==0,1, or 2
      end                // - xor  test.ul.g1 ...
    default: begin : ul
      xnor g1 (a, b, c); // if p==2 && q!=0,1, or 2
      end                // - xnor test.ul.g1 ...
  endcase
endmodule
```